CLAIMS

What is claimed is:

1. A method for forming a barrier layer on a wafer, the method comprising:

placing the wafer in a processing chamber;

powering a sputtering target for a first time period;

powering a coil for a second time period, wherein the second time period is different from the first time period; and

controlling power to both the sputtering target and to the coil during a deposition of the barrier layer.

2. The method of claim 1, wherein powering the sputtering target occurs before powering the coil and a first portion of the barrier layer formed during a time between powering the sputtering target and powering the coil is less tensile than a second portion of the barrier layer formed during a time after powering the sputtering target and powering the coil.

3. The method of claim 1, wherein powering the sputtering target and powering the coil initially occurs at approximately a same time, and wherein a power applied to the coil is reduced prior to reducing a power applied to the sputtering target, and wherein a first portion of the barrier layer formed before reducing power to the coil is more tensile than a

second portion of the barrier layer formed after reducing power to the coil.

4. The method of claim 1, further comprising powering the wafer during the deposition of the barrier layer.

5. The method of claim 1, further comprising alternately applying power and reducing power to the coil during the deposition of the barrier layer.

6. The method of claim 1, wherein a first amount of an inert sputtering gas incorporated into the barrier layer before powering the coil and a second amount of inert sputtering gas incorporated into the barrier layer after powering the coil are different.

7. The method of claim 6, wherein the inert sputtering gas includes argon.

8. The method of claim 1, wherein material is sputtered from both the coil and the sputtering target to form the barrier layer.

9. A method for forming a tantalum barrier layer on a wafer, the method comprising:

forming a first portion of the tantalum barrier layer having a first tensile stress;

forming a second portion of the tantalum barrier layer having a second tensile stress, wherein the second tensile stress is different from the first tensile stress; and

forming a conductive material over the tantalum barrier layer wherein the conductive material comprises mostly copper.

10. The method of claim 9, wherein a first concentration of an inert sputtering gas incorporated into the first portion is less than a second concentration of the inert sputtering gas incorporated into the second portion.

11. A method for forming a barrier layer on at least one wafer, the method comprising:

coating surfaces of a processing chamber with a refractory metal nitride film;

forming a barrier layer on the at least one wafer, wherein the barrier layer consists of a refractory metal; and

after a time period, recoating the surfaces of the processing chamber with another refractory metal nitride film.

12. The method of claim 11, wherein the refractory metal nitride film includes tantalum nitride and the refractory metal includes tantalum.

13. The method of claim 11, wherein the refractory metal nitride film is formed by sputtering tantalum in a nitrogen-containing ambient.

14. The method of claim 13, wherein sputtering tantalum in a nitrogen-containing ambient is further characterized as a reactive sputtering deposition process.

15. The method of claim 11, wherein the refractory metal nitride film is formed by sputtering from a refractory metal nitride target, and the refractory metal is sputtered from a refractory metal target.

16. A method for forming a layer on a wafer, the method comprising:

placing the wafer into a chamber, the chamber having a target and a coil; and

removing a first material from the target and a second material from the coil and depositing the first material and the second material on the wafer.

17. The method of claim 16, wherein a grain size of the second material is less than approximately 50 microns.

18. The method of claim 17, wherein the first material and the second material are further characterized as a copper-containing materials.

19. The method of claim 16 wherein the first material and the second material are selected from a group consisting of copper and a copper alloy.

20. The method of claim 16, wherein a removal rate of the second material from the coil is controlled to effect a uniformity of a composite layer formed by depositing the first material and the second material on the wafer.

21. The method of claim 16, wherein the layer is a copper seed layer, and wherein the copper seed layer is formed within a dual inlaid interconnect opening.

22. A method for forming a layer on a wafer, the method comprising:

forming an opening in a dielectric layer, wherein the opening exposes an underlying interconnect, and wherein the opening has corner portions formed in regions where sidewall portions of the opening

intersect surfaces of the dielectric layer that are substantially perpendicular to the sidewall portions; and

etching the opening, wherein a first power applied to a coil is at least two times greater than a second power applied to a wafer pedestal, and wherein etching the opening rounds the corner portions.

23. The method of claim 22, wherein the first power applied to the coil is approximately three times greater than the second power applied to the wafer pedestal.

24. The method of claim 22, wherein the first power applied to the coil is approximately five times greater than the second power applied to the wafer pedestal.

25. The method of claim 22, further comprising:

forming a barrier layer in the opening after etching the opening; and

forming a copper-containing layer overlying the barrier layer.

26. The method of claim 22, wherein the opening is a dual inlaid interconnect opening.

27. A method for forming a layer on a wafer, the method comprising:

placing the wafer having an exposed barrier region into a chamber; and

securing the wafer to an underlying support member wherein securing the wafer includes using a clamp, the clamp having a contact portion that contacts the wafer and a shadow portion positioned above the wafer and adjacent the contact portion, the shadow portion being positioned at a distance less than approximately 8 mils from a surface of the wafer.

28. The method of claim 27, wherein the shadow portion is positioned less than approximately 5 mils from the surface of the wafer.

29. The method of claim 27, wherein the shadow portion is positioned less than approximately 3 mils from the surface of the wafer.

30. The method of claim 27, wherein an overhang of the shadow portion is at least 2.5 time greater than a distance of the shadow portion above the surface of the wafer.

31. The method of claim 27, wherein an overhang of the shadow portion is at least 4.0 times greater than a distance of the shadow portion above the surface of the wafer.

32. The method of claim 27, wherein the clamp prevents formation of the layer over an alphanumeric identification region of the wafer.

33. A method for forming a layer on a wafer, the method comprising the steps of:

placing the wafer onto a pedestal within a chamber, wherein the chamber includes an isolation ring positioned around a periphery of the pedestal, and wherein the pedestal is biased to a first bias power; and

biasing a second region of the chamber to a second bias power, wherein the isolation ring electrically decouples the first bias power from the second bias power, and wherein portions of the isolation ring exposed to a chamber environment during forming the layer are coated with a conductive material prior to forming the layer on the wafer.

34. The method of claim 33, wherein the conductive material is aluminum.

35. The method of claim 34, wherein the aluminum is flame sprayed onto the isolation ring.

36. The method of claim 33, wherein the isolation ring includes a ceramic material.

37. The method of claim 33, wherein the second bias power is a ground potential.

38. A method for forming a copper interconnect, the method comprising the steps of:

placing a wafer into a first processing chamber, the wafer containing a dual inlaid interconnect opening having corners;

performing a preclean operation on the wafer, wherein a power applied to a coil of the first processing chamber is at least two times a power applied to the wafer, and wherein the corners of the dual inlaid interconnect opening are rounded;

transferring the wafer from the first processing chamber to a second processing chamber;

depositing a barrier layer over the dual inlaid interconnect opening, whereby a first portion of the barrier layer is formed having a first tensile stress and a second portion of the barrier layer is formed having a second tensile stress, wherein the

first tensile stress is different from the second tensile stress;

transferring the wafer from the second processing chamber to a third processing chamber; and

depositing a copper seed layer onto the barrier layer, wherein during depositing the copper seed layer, the wafer is clamped within the third processing chamber via a clamp, the clamp having a shadow portion with a height that is less than 8 mils above a top surface of the wafer.

39. The method of claim 38 wherein the clamp covers an alphanumeric identification region of the wafer, wherein no copper seed layer is formed over the alphanumeric identification region.

40. The method of claim 38, wherein the first portion and the second portion of the barrier layer are formed by altering a power provided to a coil within the second processing chamber over time.

41. The method of claim 38, wherein the copper seed layer is formed in the third processing chamber by sputtering material from both a coil within the third processing chamber and a target within the third processing chamber.

42. The method of claim 41, wherein the coil within the third processing chamber comprises copper having a grain size of less than 50 microns.

43. The method of claim 38, wherein the second processing chamber contains a dielectric isolation ring that has been at least partially coated with an adhesion layer which improves adhesion of the barrier layer to the dielectric isolation ring.

44. The method of claim 38 wherein, prior to the step of depositing the barrier layer, the second processing chamber is coated at least partially with a refractory metal nitride layer.

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